Q5 "between paragraphs 0007 and 0008 is entered 0006". This result is achieved by one of (the) channels of (the) multielemental structures on each of (the) sides of (the) said substrate is thicker than other channels, (and this) said channel is connected to a separate electrode.

Q6 "paragraph 0008". The offered transistors (offered) can be applied for a production, a transfer and a use of an electric energy within a very broad range of power: from (the) a control of an electrical soldering to (the) a control of most powerful turbogenerators. They are effective for designing electronic transformators, power supply units, and "flexible transfers of alternating current". In the latter case transistors can be connected in series, which will allow to easily create a high voltage system with operating voltage 10.sup.6 V and over with a control with light signals. These transistors can be most widely used in (the) a devices aimed at defending people from an electric shock. They can also be used in systems with (the) a unipolar power supply transmitting energy in both directions – (both) from a source to a load and from (a) the load to (a) the source. It will make it possible to increase a circuit efficiency with (the) a voltage drop between (a) the drain and the source of the open transistor not exceeding 0.5 V and, if necessary, it can be close to zero.

Q7 "between paragraph 0008 and 0009". For manufacturing offered transistors use a lightly doped substrate of monocristalline silicon with large life time. In on-state of the transistor a hole concentration near the source essentially higher than one near the drain (trapezioidal distribution) so a hole current consists of two parts: a hole diffusion, directed from the source to the drain and a hole drift, directed from the drain to the source. The hole current equals zero (zero approximation). An electron concentration approximately equals the hole concentration. An electron diffusion current and an electron drift current direct the same direction – from the drain to the source. So almost all current is transfered by electrons. Small hole current is at the expense of recombination holes and electrons in the source and smaller one is at the expense of recombination in the drain. Big hole currents flow through gates at a switching over of the transistor only. At an opening of the transistor by emission of holes from the gates to lightly doped area and accumulating of holes. At a closing one by discharge of holes (extraction).

Q8 "paragraph 0009". The structure of the offered transistor (offered) is symmetric which means that on each of (the) sides of a lightly doped n-type substrate with the impurity concentration being 10.sup.14 cm.sup.-3, there are areas of p+-gate, a n+-source and n-channel as well as electrodes of gate and source (drain). Owing to the structure symmetry, (the) a output voltage-current characteristics of the transistor are symmetric and are in the first and the third quadrants. Because of this, the source and the drain of the transistor can change places and transistor can operate in alternating voltage circuits of supply pressure of (220) 120 V and over which simplifies designing of many circuits and besides, can be applied in (the) a circuits which cannot be produced with any other types of transistors.

"paragraph 0010" (Though the structure of the transistor is symmetric the operating duty of the channel that is near the drain of the transistor essentially differs from the operating duty of the channel that is near its source. The electrical field reduces the concentration of holes in the former and increases their concentration in the latter. Owing to this, the hole concentration along an axis perpendicular to surface is trapezioidal in zero approximation. It puts certain restrictions both on the design parameters of BSIT and on designing of circuits in which these transistors are applied.) Algorithm of control of the offered transistor (offered) under typical circumstances is more complicated than that of the transistor described above ([1]) [2]. To achieve optimum characteristics three rather than two different levels voltages should be applied to the transistor gates. One of (the) voltages to the gate is about zero relatively to the nearby source, with the transistor channel closed, while the voltage applied to the gate near the drain should be about 0.4 V with the channel slightly open and the gate emit(ting) very low hole current to the lightly doped area. When changing polarity of the voltage applied, the source and the drain change places, and (the) voltages to (the) gates should be changed accordingly so as transistor is to remain closed. In this case the transistor can maintain voltages up to several kilovolt depending on parameters of the lightly doped area. Another voltage on the gate is about 0.8 V relatively of the (sourse) source and the drain which are nearby. It provides the opening of the channel and hole emission to the lightly doped area. The emission of holes to the lightly doped area is followed by electrons from the transistor source which makes the hole concentration and electron concentration practically the same in the zero approximation and may reach the magnitude of 10.sup.17 ÷ 10.sup.18 cm.sup.-3; resistance of the transistor drops sharply due to conductivity modulation and the voltage between the drain and the source of the transistor does not exceed 0.5 V at current density ≈1000 a cm.sup.-2. The level of 0.4 V can be substituted by smoothly lowering voltage on the gate which is near the source of the transistor during the switching of the transistor from on condition to off condition.

" between paragraph 0010 and 0011" In pulse duty current density can be bigger in some times, achieving 10000 a cm.sup.-2. Offered transistors, as the transistor [2],can switch over power bigger than any other types transistors all over the world.

"paragraph 0011" To have completely controllable transistor (without latch), the offered BSITs (offered) should have the channel with a low resistance. To this end, thickness of the channel should be small and the impurity concentration near the gate should be high enough so that the electronic current flowing near the gate could not cause a large voltage drop which, in turn, could lead to emission of holes. To meet these requirements, it is desirable to growth an epitaxial layer with donor impurity concentration being about 10.sup.17cm.sup.-3 on the surface of the lightly doped substrate having the donor impurity concentration about 10.sup.14 cm.sup.-3, and to have an equipment with higher resolution than is generally used for manufacturing other BSITs .On the surface of a monocristalline silicon a layer of a polysilicon may be disposed that would help to form the elements of the transistor: the gate, the source, the channel and (the) electrodes.

"paragraph 0012" The control signals on (the) gates of the transistor should depend on a polarity of the supply voltage (as a rule, it is alternating voltage with the frequency 50-60 Hz) and on the voltage supplied at (the) this moment to the transistor; to do so, it is desirable to introduce to the transistor structure two normally-on transistors with small (saturation) current which help to (fix) determine a value and the polarity of the voltage on the transistor at (that) this moment. Signals from these transistors are transmitted to the control circuit which produces control signals to (the) gates.

"paragraph 0014" In a zero approximation, the offered transistor (offered) does multiplication of voltages applied to (the) transistor gates and drains and can be considered as a double-band modulator and be used, for example, to control polarity of a rectified voltage.

brief description of the drawings

"paragraph 0019". Inventions is explained with (three) ~~eight~~ five drawings.

"between paragraph 0019 and 0020" Fig.1,2 represent a bipolar static induction transistor structure (prior art).

"paragraph 0020" Fig.(1)3 represents a bipolar static induction transistor structure.

"between paragraph 0020 and paragraph 0021" Fig.4 represents a power normally-off transistor structure with two lowpower normally-on transistors.

Fig.5 represents a bipolar static induction transistor structure with epitaxial layers.

Fig.6 represents a power normally-off transistor structure with two lowpower normally-on transistors disposed in epitaxial layers.

"paragraph 0021" Fig.(2) 4 represents a symbolic image offered of the transistor.

"paragraph 0022" Fig.(3) 8 represents a symbolic image offered of the power normally-off transistor with two lowpower normally-on transistors.

detail description of the preferred embodiment

"between paragraphs 0022 and 0023". A bipolar static induction transistor fig.1 comprises substrate 1,drain electrode 2,epitaxial layer 3,gate 4, gate electrode 5, source 6,channel 7,source electrode (n+-type polysilicon)8,source contact 9.

A bipolar static induction transistor fig.2 comprises substrate 10,drain electrode 11,epitaxial layer 13,gate 14, gate electrode 15, source 16,channel 17,source electrode (n+-type polysilicon) 18,source contact 19,isolation 20.

"paragraph 0023" The bipolar static induction transistor fig.3 comprises lightly doped n-type substrate (1) 21, gate electrodes (2) 23, gates (3) 22, source and drain electrodes (n.sup.+-type polysilicon) (4) 26, (drain electrode 5) source and drain contacts 27, channels (6) 25, source and drain (7) 24.

"between paragraphs 0023 and 0024" The bipolar static induction transistor fig.4 comprises lightly doped n-type substrate 28,gates 29, gate electrodes 30, thick channels 31,thick channel electrodes 32,source and drain 33,channels 34,source and drain electrodes (n+-type polysilicon) 35,source and drain contacts 36,thick channel contacts 37.

The bipolar static induction transistor fig.5 comprises lightly doped n-type substrate 38,epitaxial layers 39,gates 40, gate electrodes 41, source and drain 42,channels 43,source and drain electrodes (n+-type polysilicon) 44,source and drain contacts 45,isolation 46.

The bipolar static induction transistor fig.6 comprises lightly doped n-type substrate 47,epitaxial layers 48,gates 49, gate electrodes 50, thick channels 51,thick channel electrodes (n+-type polysilicon) 52, thick channel contacts 53,ordinary channels 54,source and drain 55,source and drain electrodes 56,source and drain contacts 57, isolation 58.

"paragraph 0024" The symbolic image of the transistor fig.7 comprises gates (8,9) 59,60; source and drain(s sources) ~~(10~~,11) 61, 62.

"paragraph 0025" The symbolic image of the power normally-off transistor with two lowpower normally-on transistors fig.8 comprises gates (12,13) 63,64; source and drain(s sources) of lowpower transistors (14,17) 65, 68; source and drain(s sources) of a power transistor (15,16) 66,67.

"paragraph 0026" The offered transistor (offered) can be named "symmetric channel tetrod".

"paragraph 0027" is canceled.

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3. Smoliansky B.A. et al. Author's certificate USSR №736807.Transistor. H01L 29/70. Priority 22.01.1979.